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Portable library of migratable sockets

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Abstract:

Efficient load balancing is essential for parallel distributed computing. Many parallel computing environments use `{\tt TCP}` or `{\tt UDP}` through the socket interface as a communication mechanism. This paper presents the design and development of a prototype implementation of a network interface that can preserve communication between processes during process migration. This new communication library is a substitution for the well-known socket interface. It is implemented in user – space; it is portable, and no modifications of user applications are required. `{\tt TCP/IP}` is applied for internal communication, which guarantees relatively high performance and portability.

Keywords:

distributed computing load balancing process migration `{\tt Dynamite}` sockets


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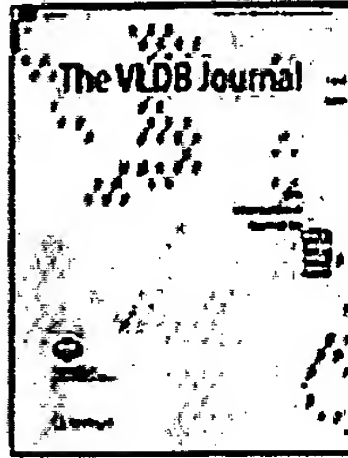
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Designing wrapper components for e-services in integrating heterogeneous systems

Massimo Mecella ^{A1} and Barbara Pernici ^{A2}^{A1} Università di Roma "La Sapienza", Dipartimento di Informatica e Sistemistica, Via Salaria 113, 00198 Roma, Italy; E-mail: mecella@dis.uniroma1.it^{A2} Politecnico di Milano, Dipartimento di Elettronica e Informazione, Piazza Leonardo da Vinci 32, 20133 Milano, Italy; E-mail: barbara.pernici@polimi.it

Abstract:

Component-based approaches are becoming more and more popular to support Internet-based application development. Different component modeling approaches, however, can be adopted, obtaining different abstraction levels (either conceptual or operational). In this paper we present a component-based architecture for the design of e-applications, and discuss the concept of wrapper components as building blocks for the development of e-services, where these services are based on legacy systems. We discuss their characteristics and their applicability in Internet-based application development.

Keywords:

Key words: e-service - e-application - Component - Wrapper - Legacy system - Cooperation - Integration

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Object Wrapper: An Object-Oriented Interface for Relational Databases

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Abstract

Most commercial applications have to cope with a large number of stored object instances and have data shared among many users and applications. For object-oriented as well as conventional application development RDBMS technology is currently being used in most case. We describe a software module called Object Wrapper for storing and retrieving objects in a RDBMS. Having these capabilities in a separate component helps to isolate data management system dependencies and hence contributes to portable applications.

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Abstract

This paper describes techniques for reducing test station hardware dependence in test programs in National Instrument's LabVIEW development environment hardware dependence is reduced by design strategies, and by the definition of a Hardware Abstraction Layer (HAL). The HAL reduces dependence by insulating the developer from the test station resources, by encapsulating the hardware supplied by the equipment manufacturer with wrapper functions. The HAL allows the TPS to be hardware dependent and independent components, localizing the hardware dependencies in the test program. This paper also describes a method using hardware configuration tables to effectively defer hardware resources until program execution. This technique allows the TPS to compensate for minor hardware configuration without having to edit or recompile any LabVIEW code.

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↑ INDEX TERMS

Primary Classification:

D. Software

↳ D.3 PROGRAMMING LANGUAGES

↳ D.3.4 Processors

↳ **Subjects:** Compilers

Additional Classification:

D. Software

↳ D.3 PROGRAMMING LANGUAGES

↳ D.3.2 Language Classifications

↳ **Nouns:** C++

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↑ ABSTRACT

Many useful programming language extensions and system support libraries require knowledge of the locations of fields within objects at run time. Examples include orthogonal persistent object stores, precise garbage collectors, data structure picklers, and parameter marshaling schemes. For clean and efficient implementation as libraries, these systems require run-time knowledge of in-memory layouts of data objects, which is unavailable in most traditionally compiled and linked programming languages, such as C, C++, and Ada. Even the recently standardized *run-time type identification* (RTTI) feature in C++ is insufficient, because it describes only language-level features of the type hierarchy and not the compiler-dependent object layout decisions. We present a facility for *run-time type description*, or RTTD, which extracts low-level layout information from debugging information generated by conventional compilers, and makes it available to user programs. We believe this to be the simplest and most portable approach to run-time type description, requiring no changes to existing compilers. In this paper, we describe the basic strategies and present details of our implementation for C++. We also sketch some extensions that we have implemented, including special treatment of C++'s virtual function table pointers to match persistent or foreign data objects with the actual code in a particular application. Our implementation of run-time type description is freely available. It is in regular use with multiple operating systems and compilers, in both free and commercial products, including a high-performance persistent object storage system for C++ and a real-time garbage collector.

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Anjo, K. Okamura, A. Kajiwara, T. Mizushima, N. Omori, M. Kuroda, Y.
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Abstract

An NECoBus (internal code name), a bus architecture designed for creating portable yet high-throughput SOC's, is described. Its distinguishing feature is a wrapper-based NECoBus Core Interface (NCI) mechanism: an IP core is designed to communicate with another through the NCI, where the NECoBus includes wrappers to hide bus protocols and the wiring delay from the IP core. Importantly, the NECoBus wrapper employs several latency reduction techniques that can effectively remove the latency penalty induced in the conventional wrapper-based bus design: (1) retry encapsulation, (2) write-buffer switching, (3) early bus request and (4) converter-based multiple bit-width connection. The first implementation of the 32/64 bit NECoBus that has been targeted at a 200-MHz bus cycle using the 0.13- μm CMOS processes is described in this paper. Evaluation results demonstrate a 16% throughput improvement, and a 15% and 40% read/write latency reduction by those newly developed techniques.

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